REMARKS

In response to the Office Action mailed July 6, 2004, Applicant respectfully requests reconsideration.

The Office Action indicates that the title is not descriptive. Applicant proposes to change the title to "AN ARITHMETIC UNIT FOR MULTIPLYING A FIRST QUANTITY X BY A SECOND QUANTITY Y" and believes that this title is clearly indicative of the invention to which the claims are directed. Acceptance of the proposed new title is respectfully requested.

The drawings were objected to because, according to the Office Action, Figures 1-2 and 7-8 should be labeled as "Prior Art". In response to this objection, Applicant is submitting drawing corrections with the legend "Prior Art" added to Figures 1 and 2 but is not, at this time, submitting a drawing correction with respect to Figure 7-8. Applicant does not believe, at this time, that Figures 7-8 should be considered "Prior Art".

Claims 1-24 were rejected under 35 U.S.C. §112, second paragraph as being indefinite. In particular, the Office Action pointed to language in claims 1, 17, and 18 as requiring clarification. In response to this rejection, Applicant has amended claims 1, 17, and 18 to overcome the indefiniteness rejection and the claims should now be clear enough to satisfy the statute. Accordingly, withdrawal of the rejection under 35 U.S.C. §112, second paragraph, is respectfully requested.

Claims 1, 8, 16, 19, and 23-24 were rejected under 35 U.S.C. §102(e) as being anticipated by Vo. Applicant respectfully disagrees with this rejection.

Vo describes a multiplier circuit that generates a negate product –X*Y without requiring a separate negate operation. Vo uses bit pair recoding in a Booth algorithm to perform a rapid multiplication or negate multiplication operation. The process parses the second value string into a series of lengths, which are encoded into a known bit pair code as shown in Figure 3A. These bit pair encoded strings can be paired to indicate plus or minus index multiples which are then used to generate the partial product in the partial product multiplier. As shown in Figure 3A, the first two bits of the encoded multiplier string 304 indicate whether or not the multiplier string has a value of –2 or 2 or an index of $+2^1$ or -2^1, the next two bits indicate whether the multiplier string has the value of –1 or +1 (or an index of $+2^0$ or -2^0), and the final encoded multiplier string

bit indicates whether or not the multiplier string has the value of zero. Therefore, in such a system, in order to encode three bits of the multiplier string, five bits are required to form the code.

By contrast, claim 1 recites an arithmetic unit for multiplying a first quantity X by a second quantity Y, said arithmetic unit comprising: a Booth coder having a plurality of inputs for receiving a plurality of bits of the second quantity and a plurality of outputs for providing Booth coded outputs; circuitry connected to at least one of said inputs for receiving one of said plurality of bits of the second quadrant and said outputs for providing Booth coded outputs, said circuitry comprising a further input to receive a signal indicating if a multiply accumulate or multiply subtract function is to be performed, said circuitry arranged to modify at least one output of the coder if necessary in accordance with said signal, whereby the output of said Booth coder unit is a Booth coded signal modified if necessary to take into account the unction to be performed wherein said coder is arranged to provide a SIFL output, an NZP output and an NZN output. wherein said unit is capable of performing the calculations X multiplied by Y and X multiplied by Y, the output of the Booth coder being the same for both of said calculations, and a Booth decoder arranged to separate a partial product from said Booth coded signal and said first quantity.

Clearly, the three bit encoded output encoding each three bits is "arranged to provide a SNGL output, an NZP output, and an NZN output". Thus, embodiments of the present invention can use fewer multipliers to process the signal and fewer bit lines between the Booth encoder and the Booth decoder (multiplier).

Thus, claim 1 clearly distinguishes over Vo and is in allowable condition. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §102(e) is respectfully requested.

Claims 2-24 depend from claim and are allowable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Sebastien FERROUSSAT, Applicant(s)

By: _____

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Docket No.: S1022.80717US00
Date: November 5, 2004
x11/06/04x

IN THE DRAWINGS

"Replacement Sheets" are attached which includes a clean version of amended Figures 1 and 2. The attached sheets replace the original sheets including Figures 1 and 2.

DOCKET NO.: S1022.80717US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sebastien FERROUSSAT
Serial No.: 09/919,496
Conf. No.: 4821
Filed: July 30, 2001
For: AN ARITHMETIC UNIT FOR MULTIPLYING A FIRST QUANTITY X BY A SECOND QUANTITY Y (Formerly ARITHMETIC UNIT)

Examiner: Tan V. Mai
Art Unit: 2124

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 5th day of November, 2004.

Eileen MacKenzie

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REQUEST FOR APPROVAL OF PROPOSED DRAWING CORRECTIONS

Enclosed are two (2) pages of proposed drawing corrections for Figures 1 and 2. The proposed corrections are marked in red ink. The Examiner is respectfully requested to approve these proposed drawing corrections.

Respectfully submitted,

Sebastien FERROUSSAT

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Date: November 5, 2004

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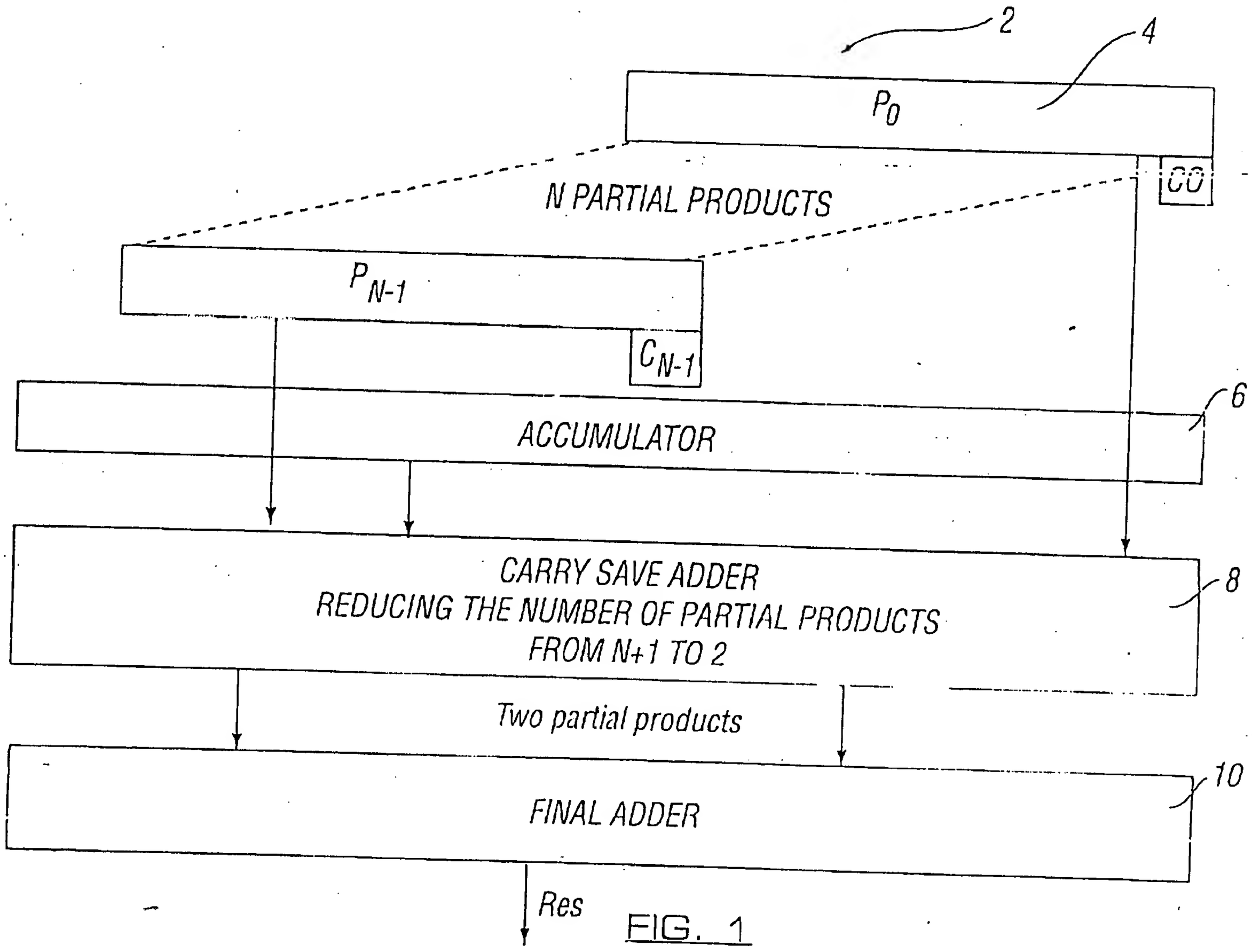

FIG. 1

Prior Art

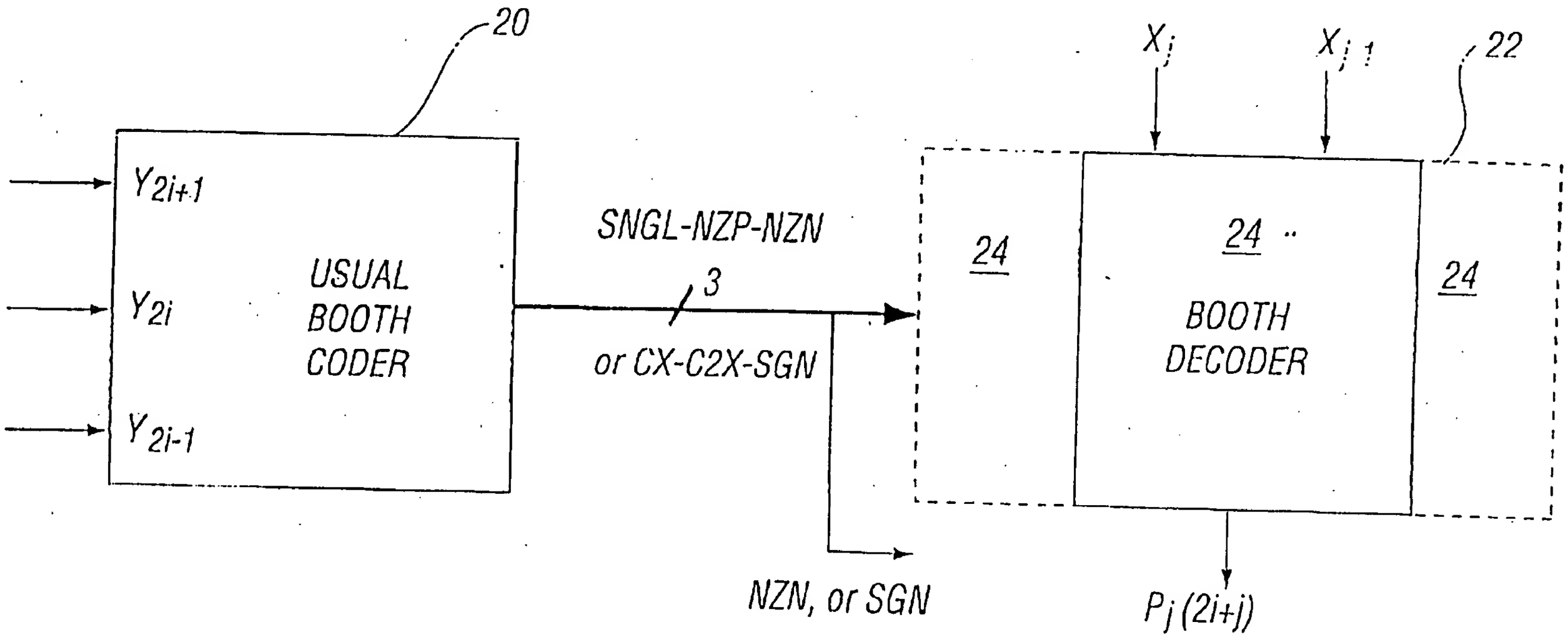

FIG. 2

Prior Art